THD Analysis for 5-Level and 7-Level Cascaded Multilevel Inverters at Varying Switching Frequencies."

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Abstract -Multilevel inverters convert DC voltage to AC voltage by using lower DC voltage at the input, with the help of an electronically controlled device. However, one of the main challenges associated with these devices is the Total Harmonic Distortion (THD) of the output waveform. In this research paper, a brief review of THD is presented for different cascaded H-bridge multilevel inverter topologies, specifically five and seven-level inverters (for example). The five-level inverter uses eight switches, while the seven-level inverter uses twelve switches. Each single H-bridge inverter circuit is fed by independent DC sources. The inverter employs an Insulated Gate Bipolar Transistor (IGBT) as the switching point and a gating block to control the operation of the IGBT switching. Simulation results and waveform analysis are presented to validate the research. The study also explores the effect of varying the switching frequency of the carrier wave on the total harmonic distortion of the output waveform. The paper emphasizes the importance of selecting an appropriate switching frequency based on the application requirements to improve the performance and efficiency of cascaded multilevel inverters.

Keywords- Multilevel inverters, Total Harmonic Distortion, cascaded H-bridge multilevel inverter topologies, single H-bridge inverter circuit, independent DC sources, waveform analysis,

I- INTRODUCTION

Multilevel inverters are electronic devices that can generate the desired alternating voltage at the output by using lower DC voltages as input. Typically, solar cells, fuel cells or batteries are used as input sources. A two-level inverter is commonly used to convert DC voltage to AC voltage, but its waveform is non-sinusoidal and contains harmonics. To overcome the disadvantages of the conventional two-level inverter such as low efficiency, high cost and switching losses, multilevel inverters have been introduced. Multilevel inverter systems are capable of generating a pure sinusoidal waveform of different levels at the output voltage, as shown in Fig.(1), this topology is increasingly popular for its high voltage operating capabilities, relatively low switching losses, high efficiency and low Electromagnetic Interference (EMI). It has received significant attention across multiple disciplines in recent years due to its ability to generate output voltage with less Total Harmonic Distortion (THD) and suppressed harmonics while reducing the percentage of losses. The multilevel inverter topology is developed to produce an AC source that is almost similar to a pure power generation source and can be used in AC loads. By increasing the inverter circuit levels, it is possible to obtain a smooth waveform. The more the levels, the smoother the output voltage waveform will be [2,3,4].

The multilevel inverters can be classified (according to the type of DC sources) into two main types separate dc source and common dc source, the first type is divided to cascaded inverters and flying capacitors. The second type uses diode-clamped inverters. The cascaded H-bridge inverter is popularly used for single-phase systems.

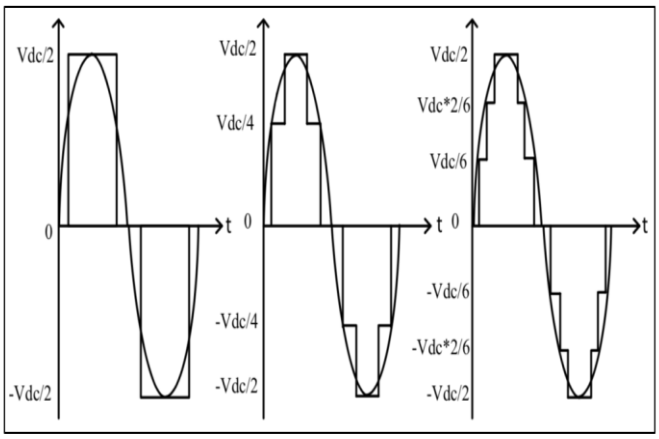


Fig. 1 Output voltage waveform for 3-level, 5 level, 7 levels of multilevel inverters [2].

The PWM-based technique can give a better dynamic response in addition to the lower THD of output voltage and current. The difference between the several topologies of multilevel inverters available in the mechanism of switching and the source of input voltage to the multilevel inverters. The three most commonly used multilevel inverter topologies are cascaded bridge multilevel inverters, Diode Clamped multilevel inverters and Flying Capacitor multilevel inverters. Among these three Cascade H-bridges multilevel has a modular structure and requires fewer components than diode clamped and flying capacitor multilevel inverter, and consequently, it is widely used for many applications. The key features of multilevel inverters are as follows [5, 6]:

1. The output voltage and power increase with numbers of level.
2. The harmonic proportion is inversely proportional to a number of levels and hence the requirement of the filter decreases.
3. The harmonic can be formerly selected for elimination as higher voltage levels have more free switching angles. .

4. Switching devices are having capacity for Static and dynamic voltage sharing. Clamping diodes or capacitors structures are helping for the same.

5. Voltage-sharing problems are not faced by the switching device [7,8]

This paper mainly focuses on the Simulation results of five-level and seven-level single-phase cascaded H-bridge multilevel inverters and the effects of the switching frequency on their THD values are presented.

II- CSCADED H-BRIDGE MULTILEVEL INVERTER

The cascaded multilevel inverter (CMI) with separated DC sources is considered the most practical topology for power conversion in medium and high-power applications. This is due to its ability to eliminate the need for bulky transformers, clamping diodes, and flying capacitors that are required by conventional multilevel inverters, multilevel diode-clamped inverters, and multilevel flying-capacitor inverters, respectively. To achieve m levels, where m = (2n+1), each phase of the cascaded multilevel inverter requires number of DC sources equal n. The power circuit of the IGBT-based PWM multilevel inverter is illustrated in Fig.(2), which consists of 2(m-1) IGBTs. Each separate DC source is linked to a single-phase full-bridge inverter. The AC terminal voltages of the different level inverters are connected in series. By using various combinations of the four switches, S1-S4, each converter level can produce three distinct voltage outputs, namely +Vdc, -Vdc, and zero. The AC outputs of various full bridge converters in the same phase are connected in series, resulting in a synthesized voltage waveform that is the sum of the individual converter outputs [9].

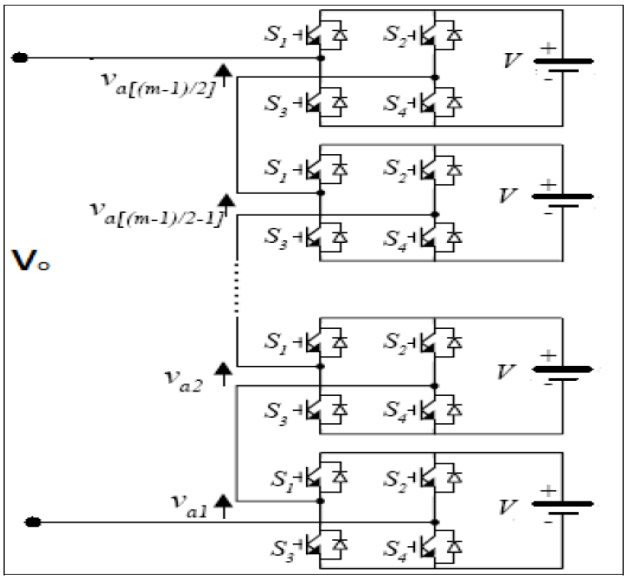


Fig.2 Single phase five-level configuration of cascaded H- bridge inverter

A) Methodology of THD Reduction

The operation of different multilevel inverters with different switching frequencies is done in the MATLAB Simulink.

Among different multilevel inverters, the five and seven-level inverter topologies introduced.

In this paper, the THD of multilevel inverters five and seven levels can be reduced by the changing the switching frequency of the carrier signals of the PWM method used. The PWM method is used to produce the desired gate pulse for the switching devices. This method requires a fewer number of components and helps reduce the harmonics of a lower order. The harmonics of a higher order will be minimized by implementing filter circuits. Basically, in the sinusoidal PWM technique, there are two signals, and one is the reference signal (sinusoidal signal) which is compared with a frequency of the higher range of the carrier signal (triangular signal), which generates the ON and OFF state. The magnitude of the voltage of output can be regulated by adjusting the modulation index (Ml). In the case of the inverter of the m-level, the triangular waves of (m−1) numbers are compared with a sinusoidal wave.

B*) Total Harmonic Distortion (THD) Calculation*

As introduced in the first chapter, the total harmonics distortion (THD) is mathematically given by

$$D = \frac{\sqrt{\sum_{n=2}^{\infty} H(n)^2}}{H1} \qquad (1)$$

Where: $H1$ is the amplitudes of the fundamental component, whose frequency is ω_0 and $H(n)$ is the amplitudes of the nth harmonics at $n\omega_0$

The amplitude of the fundamental and harmonic components of the quarter-wave symmetric multilevel waveform can be express as:

$$h_n = \frac{4E}{n\pi} \sum_{k=1}^{S} cos(n\alpha_k) \qquad (2)$$

Let $H_{(n)}=h_n$ and $H_1=h_1$

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} h_{\cdot} n^2}}{h_1} \qquad (3)$$

$$THD = \frac{\sqrt{\sum_{n=(\frac{1}{n}\sum_{k=1}^{S} Cos(n\propto_k)^2}}{\sum_{k=1}^{S} Cos(\propto_1)} \qquad (4)$$

Therefore, output voltage THD of the presented waveform can be calculated. Theoretically, to get exact THD, infinite harmonics need to be calculated. However, it is not possible in practice. Therefore, certain number of harmonics will be given. It relies on how precise THD is needed. Usually, = 63 is reasonably accepted.

III- SINUSOIDAL PWM TECHNIQUE

This technique involves generating pulses of unequal widths during a half cycle, where the pulse width is a sinusoidal function of the angular position of each cycle. To achieve this, a triangular wave and a sinusoidal waveform of the same frequency as the input voltage are compared, as

shown in Fig. (3). The pulse width modulation (PWM) type and the number of pulses per half-cycle can be adjusted to eliminate or reduce lower order harmonics. Although higher order harmonics may increase, they can be easily eliminated by filters. The number of pulses per cycle is determined by the ratio of the triangular carrier frequency to that of the modulating sinusoidal frequency. The formula for modulation index is shown in equation

$$\text{Modulation index} = A_r/A_c \quad (5)$$

A_r: amplitude of reference waveform

A_c: amplitude of carrier waveform

In case of multilevel inverter the number of carrier signals is determined by the number of output-phase voltage levels. N_c=N-1 where

N_c: number of carrier signals

N: number of output- phase voltage levels

For seven level, six carrier signals are to be used, for nine levels, eight carrier signals are to be used.

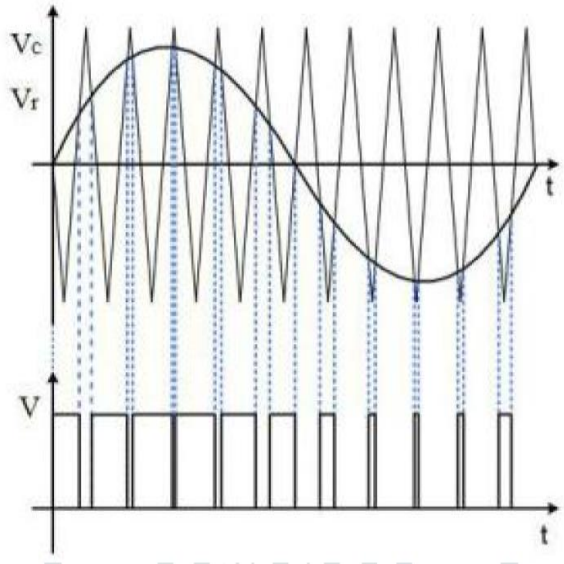


Fig.3 Concept of sinusoidal pulse width modulation

Sinusoidal Pulse Width Modulation (SPWM) is a simple fashion that is used to a sequence of voltage beats by consequent turning on/ off of power electronic switches in a motor [10]. This fashion results in generating beats of constant breadth but with varying range. The fashion involves comparing a reference sine swell with a high frequency triangular carriers. The instants of switching and commutation of the switches is determined by the points of crossroad of reference and carrier swells. For multilevel inverters, SPWM fashion is further classified as follows depending on the demand of multiple carrier signals [11,12].

1- Phase shifted pulse width modulation (PSPWM)
2- Level shifted pulse width modulation (LSPWM)
3- Phase disposition (PD)
4- Phase opposition disposition (POD)
5- Alternate phase opposition disposition (APOD) [12].

IV-HARMONIC REDUCTION TECHNIQUE

Multilevel inverters that use carrier-based modulation schemes can be divided into two categories: phase-shifted and level-shifted modulations, as illustrated in Fig. (4). Both modulation schemes are applicable to cascaded H-bridge inverters, but the total harmonic distortion of phase-shifted modulation is higher compared to level-shifted modulation. Therefore, we have chosen to use level-shifted modulation. To implement an m-level multilevel inverter using level shifted multicarrier modulation, (m-1) triangular carriers with the same frequency and amplitude are required. The (m-1) triangular carriers are arranged vertically in such a way that the bands they occupy are contiguous. The frequency modulation index, given by mf = f_{cr}/f_m, remains the same as that for the phase-shifted modulation scheme, while the amplitude modulation index is defined as:

$$ma = \frac{Vm}{Vcr(m-1)} \quad \text{For} \quad 0< ma<1 \quad (6)$$

Where Vm : is the peak amplitude of the modulating wave
Vcr : is the peak amplitude of each carrier wave.

The Level shifted pulse width modulation has three types named as:
1- In-phase Disposition (IPD),
2-Phase opposition disposition (POD)
3- Alternate phase opposition disposition (APOD)
(a) In-phase disposition (IPD), where all carriers are in phase.
(b) Alternative phase opposite disposition (APOD) ,where all carriers are alternatively in opposite disposition.
c) Phase opposite disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference. [13]

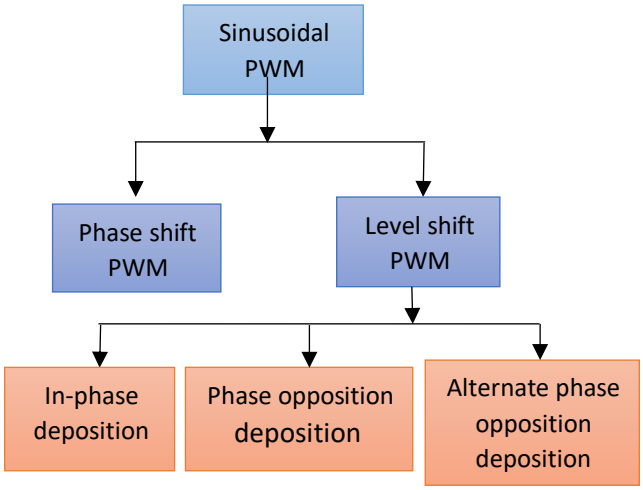


Fig.4 Classification of sinusoidal PWM used for multilevel inverter.

V- FIVE LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

The five level cascaded H-bridge inverter circuit consists of two single H-bridge inverter circuits as shown in Fig.(5). Each H-bridge circuits been supply with DC voltage as input giving a total of two inputs (V1 and V2). Each single H-bridge consist of four IGBT, total of eight switches for all stage cell (S1, S2, S3, S4, S5, S6, S7 and S8) in arrangement of H shape and each IGBT connected with one gating block for switching IGBT. The cascaded H-bridge inverter circuit has 100V DC supply into each single H-bridge inverter circuit. Every IGBT assigned with individual gating parameters for switching purposes to produce suitable waveform pattern. To obtain the desired level in output voltage for five level inverter, switches are operated according to table (1). It is apparent from the table (1), that the 'ON' and 'OFF' state for the switches are represented by both 0 and 1. In each output voltage line for this inverter, four IGBT need to be turn 'ON' while remaining four will remains 'OFF'.

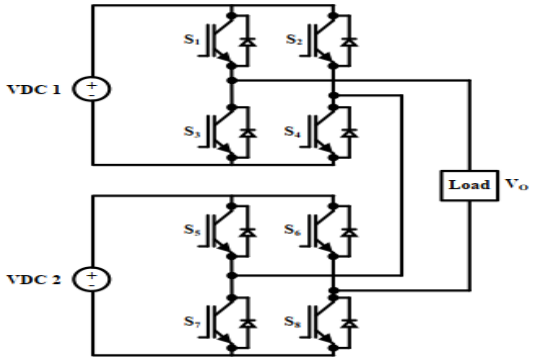


Fig. 5 Single phase structure of a five- level cascaded H-bridge inverter.

Table 1. output voltage levels for the five levels of multilevel inverter

S1	S2	S3	S4	S5	S6	S7	S8	Voltage level
0	1	1	0	0	1	1	0	$+V_{DC}$
1	1	0	0	0	1	1	0	$+V_{DC}$
1	1	0	0	1	1	0	0	0V
1	1	0	0	1	0	0	1	$-2V_{DC}$
1	0	0	1	1	0	0	1	$-V_{DC}$

VI-SEVEN LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

To generate the desired output waveform in a seven level cascaded H-bridge inverter, three single H-bridge inverter circuits are needed, as shown in Fig.(6) . Each circuit is fed with an independent DC voltage source of the same magnitude (V1, V2, and V3) and consists of twelve IGBTs arranged in an H shape (S1-S12). The DC input voltage supply for each H-bridge cell is 100V, and each gating block produces a switch pattern as a waveform for the power IGBT. The switching operation required to obtain the output waveform for the seven level multilevel inverter is given in table (2). In this table, the 'ON' and 'OFF' states of the switches are represented by 1 and 0, respectively. It can be observed from the state changes that six switches will conduct at a time to generate the required level in each output voltage line.

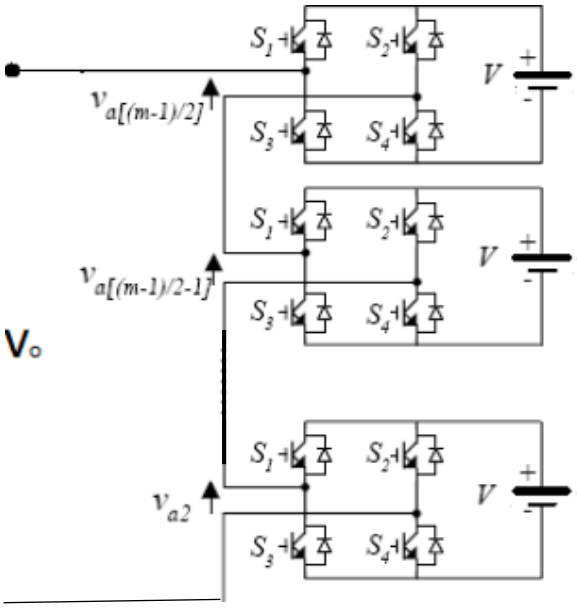


Fig.6 Single phase structure of a seven level cascaded H-bridge inverter.

Table 2. output voltage levels for the seven levels of multilevel inverter

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	Voltage level
1	0	0	1	1	0	0	0	1	0	0	1	$+V_{DC}$
1	0	0	1	1	0	0	0	0	0	1	1	$+V_{DC}$
1	0	0	1	0	0	1	0	0	0	1	1	0V
0	0	1	1	0	0	1	0	0	0	1	1	$-2V_{DC}$
0	1	1	0	0	0	1	0	0	0	1	1	$-V_{DC}$
0	1	1	0	0	1	1	1	0	0	1	1	
0	1	1	0	0	1	1	1	0	1	1	0	

VII- ANALYSIS FOR SINGLE PHASE CASCADED H-BRIDGE

In order to examine the ability of both five level and seven level cascaded H-bridge inverter to generate all possible positive and negative level symmetrically in output voltage waveform, both been set with different value of switching angle. For simulation purposes, each value of DC voltage sources is 100V and frequency of output voltage are assumed to be 50Hz .The load resistance is 5 Ohm and 5mH inductance. Voltage of different levels (five and seven) are analyzed and for calculation of harmonics, help of FFT analysis is taken and THD is determined and presented for different cases of carrier frequency and different levels in figures below.

(A) Output Voltage for Five Level and Seven Level Multilevel Inverter

Figures (7,8) show the Matlab/Simulink for five and seven level multilevel inverters respectively. Output voltage for five level and seven level inverter is shown in Fig. (10) and Fig. (11) and it is confirmed that the inverter could generates all desired positive and negative level symmetrically in output voltage waveform, both been set with different values of switching frequency. The maximum output voltage obtained from circuit simulation is +200V while minimum value shows -200V as seen in Figure 9.and Figure 10 show, the maximum output voltage obtained from circuit simulation is +300V while minimum value shows -300V as seen . The waveform of the output voltage can be considered by configuring the value of the input DC voltage. The configuration of the voltage can determine the level of the waveform.

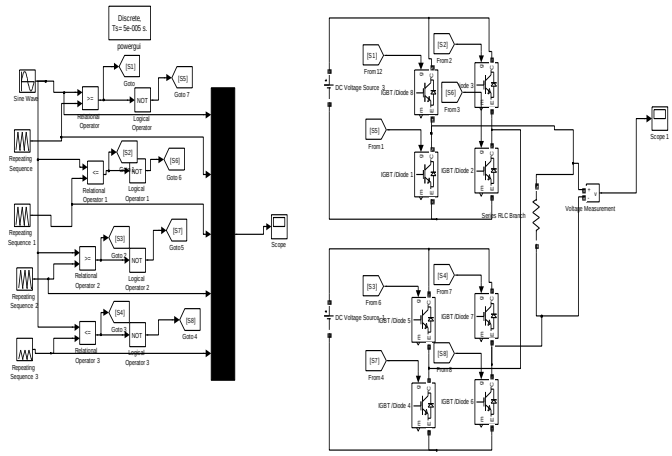


Fig.7 Matlab/Simulink for five level multilevel inverter.

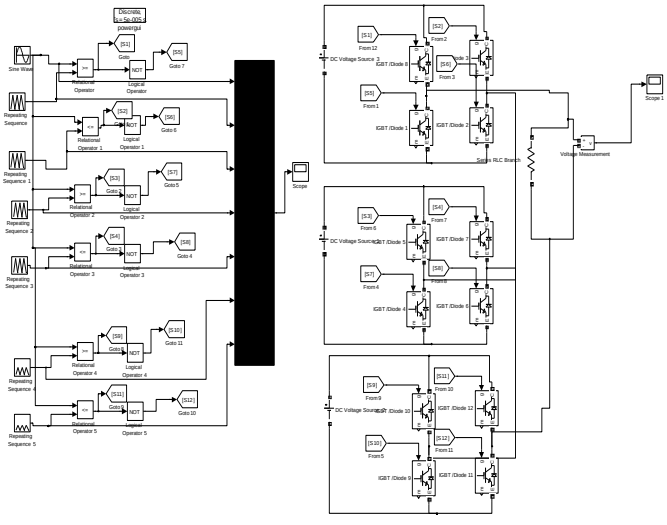


Fig.8 Matlab/Simulink for seven level multilevel inverter

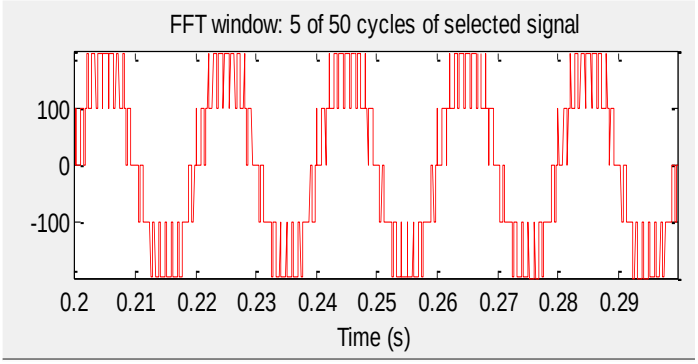


Fig.9: The output voltage waveform for five- level inverter

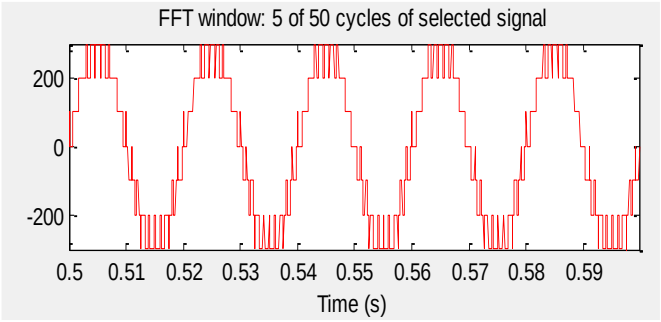
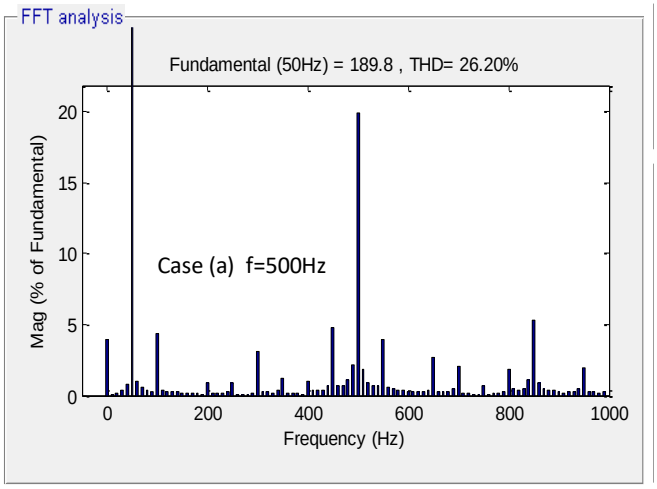
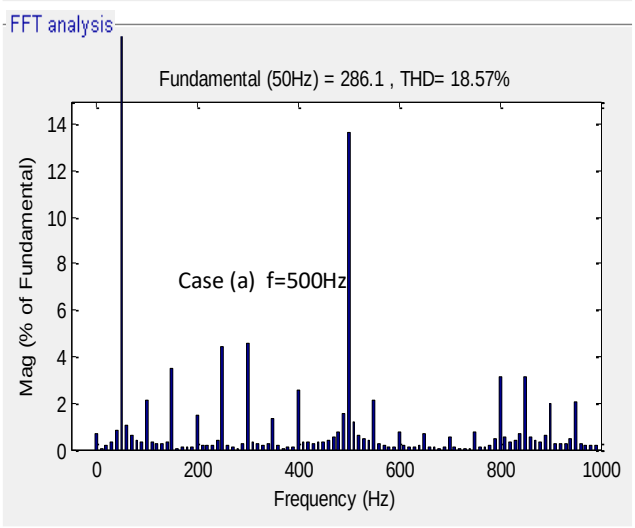


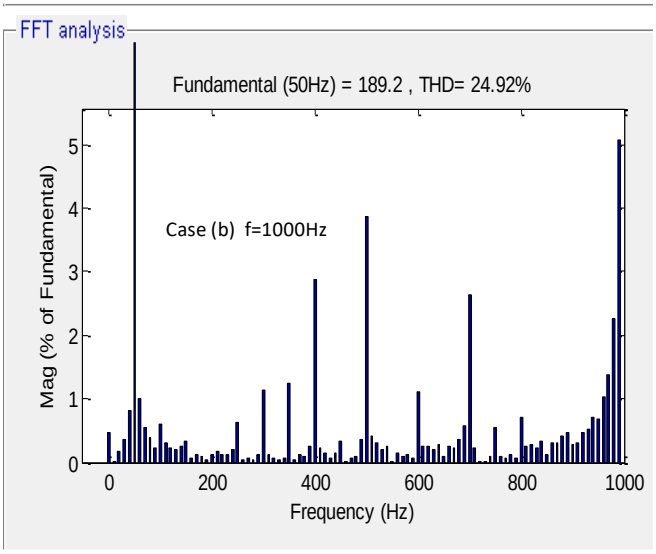
Fig. 10 The output voltage waveform for seven -level inverter

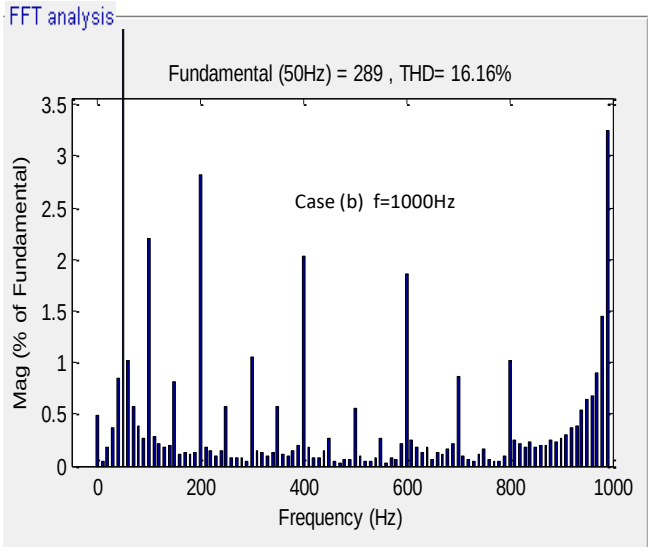
(B) THD in Five Level and Seven Level Multilevel Inverter at Different Switching Frequency.

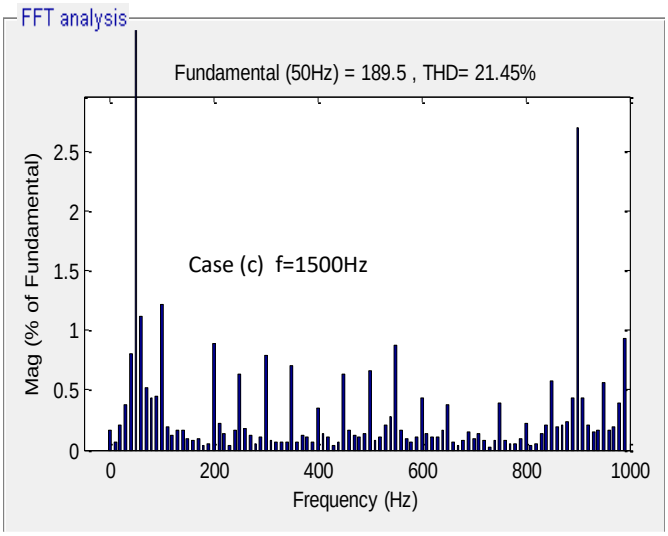
Since it is the purpose of the inverter to use a DC voltage source to supply load required an AC, the quality of the AC output voltage or current should be described in terms of THD. The simulation results for THD at different switching presented. Figure 11 shows the THD for the output voltage of five level multilevel inverter at switching frequency 500, 1000, 1500, 2000 and 2500Hz respectively. From this figure, we note that at f=500Hz, THD is 26.2%, and at f=1000Hz, the THD is 24.92%, at f=1500Hz, THD is 21.45%, at f=2000Hz, THD is 18.95% and at f=2500Hz, THD is 16.13%. This values indicates that, the THD of the output voltage decreased as the switching frequency increases. Figure12 shows the THD for the output voltage of seven level multilevel inverter at switching frequency 500, 1000, 1500, 2000 and 2500Hz respectively. From this figure, we note that at f=500Hz, THD is 18.75%, and at f=1000Hz, the THD is 16.06%, at f=1500Hz, THD is 14.05%, at f=2000Hz, THD is 12.12% and at f=2500Hz, THD is 10.07%. This values indicates that, the THD of the output voltage decreased as the switching Frequency increases. It can be deduced also that, for five level at f=5000Hz, THD is 26.2$ but for seven level at the same frequency, THD is 18.57% and at f=1000Hz, THD for five level is 24.92% , but for seven level THD is 16.06%. At f=1500Hz, THD of five level is 21.45% and for seven level THD is 14.05%. At f=2000Hz, THD for five level is 18.95% and for seven level THD is 12.12%. At f=2500Hz, THD for five level is 16.13% but for seven level THD is 10.07%











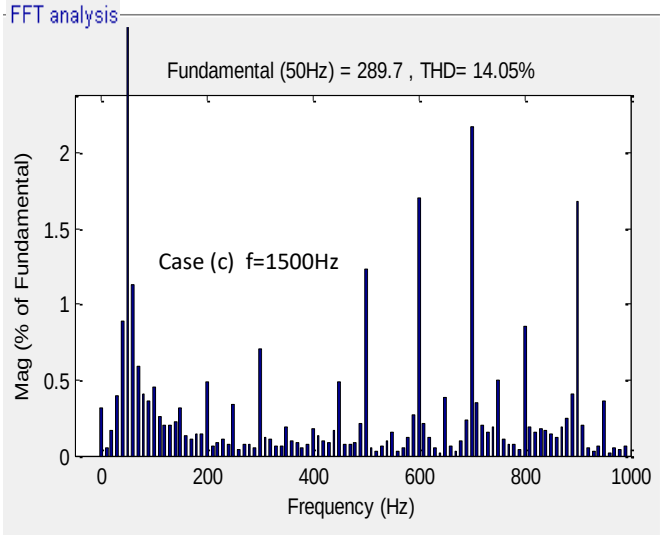


Fig. 11: THD of the voltage waveform for five level at (a) 500, (b)1000, (c)1500 Hz

Fig.12: . THD of the voltage waveform for seven level at (a) 500, (b)1000, (c)1500 Hz

Table (3) Statistical values of the THD of the voltage waveform for different cases of study with different frequencies and levels

THD (Total harmonic distortion)				Frequency Hz
11-level	9-level	7-level	5-level	
10.13	12.29	18.75	26.2	500 Hz
8.73	12.2	16.06	24.92	1000 Hz
7.43	10.87	14.05	21.45	1500 Hz
7.02	9.84	12.21	18.95	2000 Hz
6.3	9.13	10.76	16.13	2500 Hz
5.23	8.13	9.28	13.72	3000 Hz
4.34	7.88	7.49	11.16	3500 Hz
3.69	7.65	6.59	10.6	4000 Hz
3.1	7.12	6.3	8.13	4500 Hz
3.01	7.1	5.47	8.01	5000 Hz

On the other side results in better THD values for increasing switching frequency but increased the power switching losses [13] FFT results of five-level, seven-level, nine-level, and eleven-level multilevel inverter gives total harmonic distortion of four configuration in case of varying the switching frequency are shown in table (3). It can be deduced from this analysis, the switching frequency has a significant impact on the performance of cascaded multilevel inverters, and the main effects are:

1. Output voltage quality: The switching frequency affects the quality of the output voltage waveform of the multilevel inverter. As the switching frequency increases, the harmonic content of the output voltage decreases, which results in a higher quality waveform with lower total harmonic distortion (THD). However, increasing the switching frequency also increases the switching losses and the complexity of the control circuit.
2. Efficiency: The switching frequency also affects the efficiency of the multilevel inverter. At low switching frequencies, the losses due to switching and conduction in the power devices are low, but the output voltage quality is poor. Conversely, at high switching frequencies, the losses due to switching and conduction are high, but the output voltage quality is high. Therefore, the switching frequency should be optimized to achieve a balance between output voltage quality and efficiency.
3. Component stress: The switching frequency affects the stress on the components of the multilevel inverter. At high switching frequencies, the switching losses increase, which results in a higher operating temperature and thermal stress on the power devices. Additionally, high-frequency switching can result in high-frequency noise and electromagnetic interference (EMI), which can affect the performance and reliability of the inverter.
4. Control complexity: Increasing the switching frequency also increases the complexity of the control circuit of the multilevel inverter. At high switching frequencies, the control circuit needs to respond quickly to changes in the load and the input voltage, which can be challenging to implement. Additionally, the high-frequency switching can result in higher EMI, which can interfere with the control circuit and affect its performance.
5. Overall, the switching frequency has a significant impact on the performance and efficiency of cascaded multilevel inverters, and it is important to optimize the switching frequency based on the requirements of the application.

VIII- CONCLUSIONS

This paper discusses the effects of increasing the number of levels and switching frequency on the total harmonic distortion (THD) of multilevel inverters. It is concluded that higher levels and switching frequencies lead to lower THD values. The use of filter circuits can further reduce harmonics [14]. The switching frequency also affects the output voltage quality, efficiency, component stress, and control complexity of the inverter. Therefore, it is essential to optimize the switching frequency based on the application's requirements to achieve a balance between output voltage quality and efficiency.

REFERENCES

[1] U. Bashir Tayab, MD. Abdullah AL Humayun, "Operation andcontrol of cascaded H-bridge multilevel inverter with proposed switching angle arrangement techniques," Journal of Engineering Science and Technology Vol. 12, No. 12 (2017) 3148 – 3157

[2] F. Kaja Mohideen1, N.Ashbahani Mohamad Kajaan, Z. Mat, N. Mohd Nayan, M. Hafiz Arshad, " THD analysis for symmetrical five level and seven level cascaded multilevel inverter," ICE4CT 2019.

[3] P. Palanivel and S. S. Dash, "Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques," IET Power Electron., vol. 4, no. 8, p. 951, 2011.

[4] V. Singh, G. V. V. R. Babu, and V. P. Singh, "New multi-level inverter topology with reduced number of switches," in Proceedings of the International Conference on Electronics, Communication and Aerospace Technology, ICECA 2017, 2017, pp. 462–467.

[5] I. Vijayshankar Mishr, K. Mahyavanshi, A. Gautam, A. Yadav, " Single-Phase Five-Level Symmetrical Cascaded H-Bridge Multilevel Inverter With Reduces Number Of Switches". 2020 IJCRT | Volume 8, Issue April 2020 ISSN: 2320-2882

[6] Adem Y , "Design and Simulation of single-phase five-level symmetrical cascaded H-Bridge multilevel inverter with reduces number of switches," J Electr Electron Syst 7: 281.

[7] M. Shilpa N. Dehedkar , A G Thosar, " Simulation of single phase cascaded H-Bridge multilevel inverters & THD analysis," Proceedings of 2018 Conference on Emerging Trends and Innovations in Engineering and Technological Research (ICETIETR).

[8] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications, " IEEE Trans. Ind. Electron., vol 49, no. 4, pp. 724-738, 2002

[9] D. Karthikeyan, R. Palanisamy, K. Selvakumar and K. Vijayakumar, "implementation of single-phase cascaded H-bridge inverter system", journal of Engineering and Applied Science 13 (21): 8993-8998, 2018

[10] Jebastin, Savari prasanth, and Vibin bharath," harmonic analysis in multilevel inveter, " Proceedings of 4th International Conference on Energy Efficient Technologies for Sustainability– CEETS'18.St.Xavier's Catholic College of Engineering, Nagercoil, TamilNadu, India, from 5th to 7th April, 2018

[11] R. Sheba Rani, C. Srinivasa Rao, M. Vijaya Kumar, " A Review Of Modulation Schemes For Single Phase Five- Level Ascaded Multilevel Inverter,".

[12] F. Qureshi, S. Shrivastava, "study of five level inverter for harmonic elimination", International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056.

[13] T. Suneel., " Multi Level Inverters: A Review Report," International Journal of New Technologies in Science and Engineering Vol. 1, Issue. 1, Jan. 2014

[14] M. Kumar Sahu, M. Biswal, J. Mohana Rao Malla, " THD Analysis of a Seven, Nine, and Eleven Level Cascaded H-Bridge Multilevel Inverter for Different Loads", ISSN 1846-6168 (Print), ISSN 1848-5588

[15] H. Chojaa et al., "A Novel DPC Approach for DFIG-Based Variable Speed Wind Power Systems Using DSpace," in IEEE Access, vol. 11, pp. 9493-9510, 2023, doi: 10.1109/ACCESS.2023.3237511.

[16] H. Chojaa et al., "Advanced Control Techniques for Doubly-Fed Induction Generators Based Wind Energy Conversion Systems," 2022 Global Energy Conference (GEC), Batman, Turkey, 2022, pp. 282-287, doi: 10.1109/GEC55014.2022.9987088